

FIG.1A

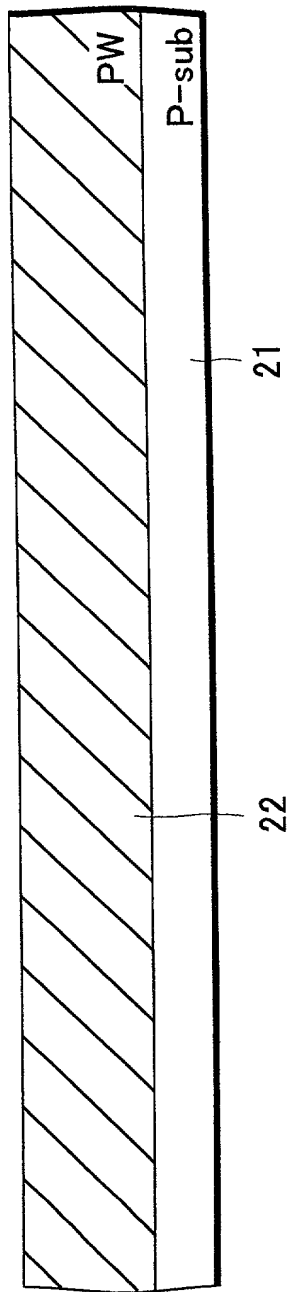


FIG.1B

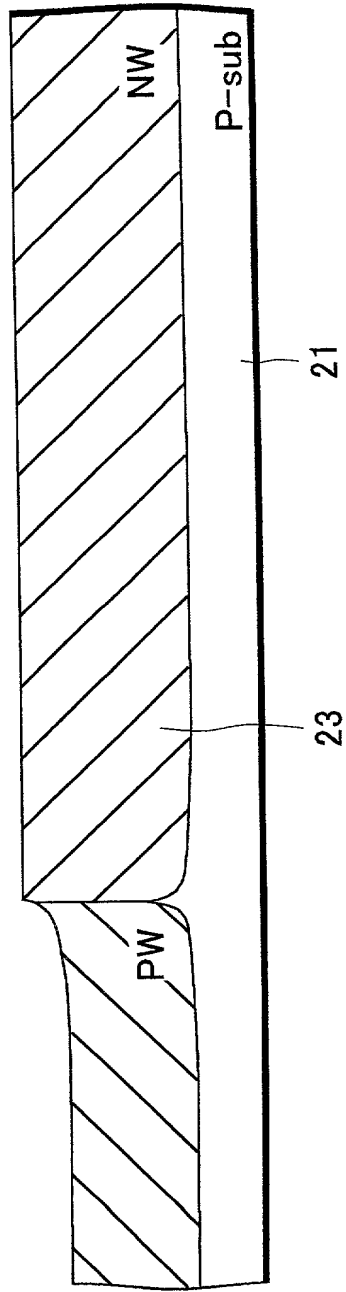
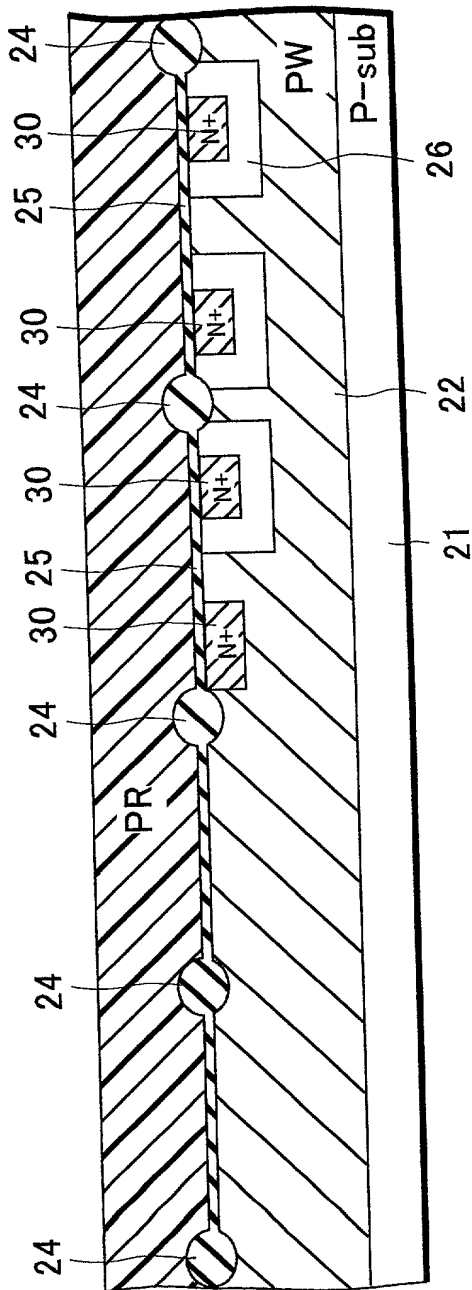


Fig. 1 is a cross-sectional view of a semiconductor device. It shows a substrate 21 with a P-sub region 22. A series of circular features 24 are arranged along a central axis, with rectangular regions 25 (labeled LN) and 26 (labeled PW) positioned between them. A label PR points to the central axis.

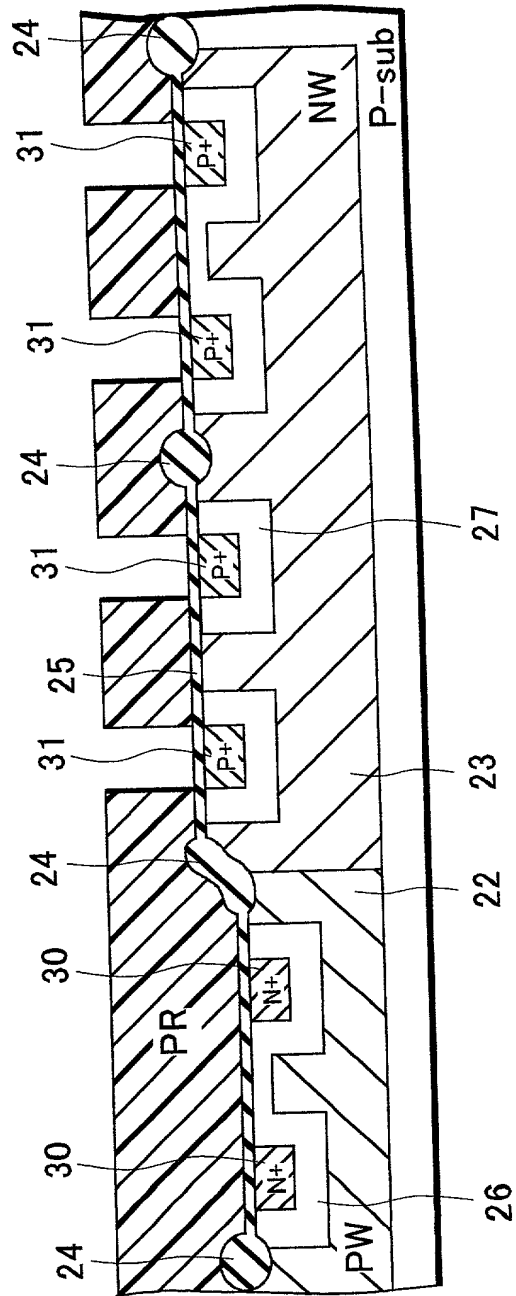
Fig. 1 is a cross-sectional view of a semiconductor device. It shows a substrate 21 with a P-sub layer 22. A series of LN (Lithium Niobate) layers 24 are deposited on the P-sub layer, separated by PR (Photoresist) layers 25. A PW (Passivation) layer 26 is shown on top of the LN layers.

[illegible]

**FIG.4A**



**FIG.4B**



[illegible]

This cross-sectional view shows a semiconductor device with a substrate 26 and a p-sub layer 33. The device features a series of gates 22, 23, 27, and 28. Contacts 24 are provided for the gates and the substrate. The gates are labeled with their respective regions: PW (p-well) for gate 22, PR (p-region) for gate 23, and NW (n-well) for gates 27 and 28. The gates are separated by spacers 30 and 31. The device is doped with N+ and P+ regions. The substrate 26 is doped with P+ and the p-sub layer 33 is doped with P+.

This cross-sectional view shows a central channel region (31) with a p-type substrate (p-sub) (27). The channel is flanked by p+ regions (24, 25) and n+ regions (26, 28). A p-well (PW) is formed in the substrate, and a p+ region (PR) is located in the channel. The device is labeled with various regions: 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100.

FIG. 7A

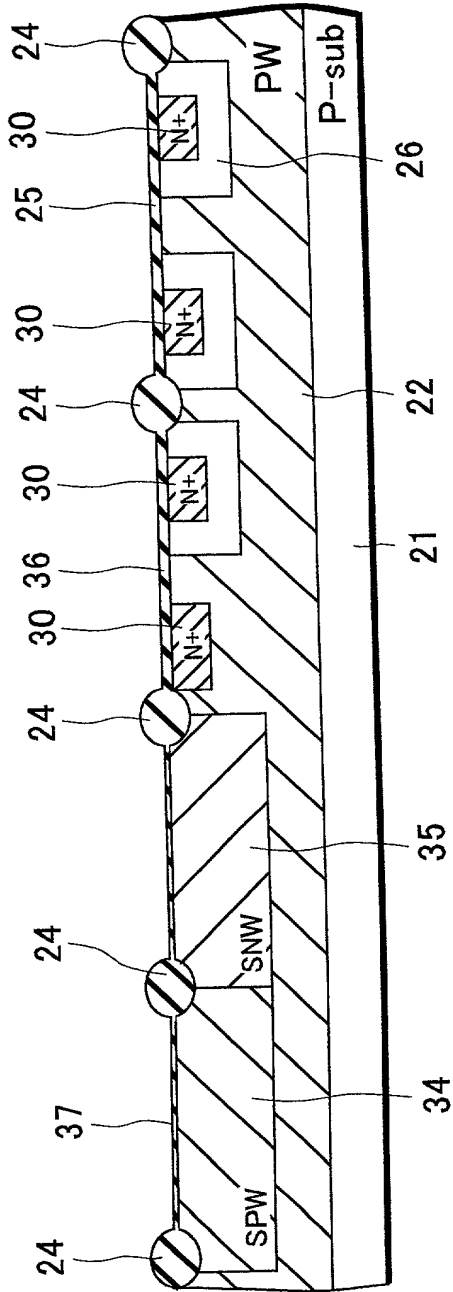
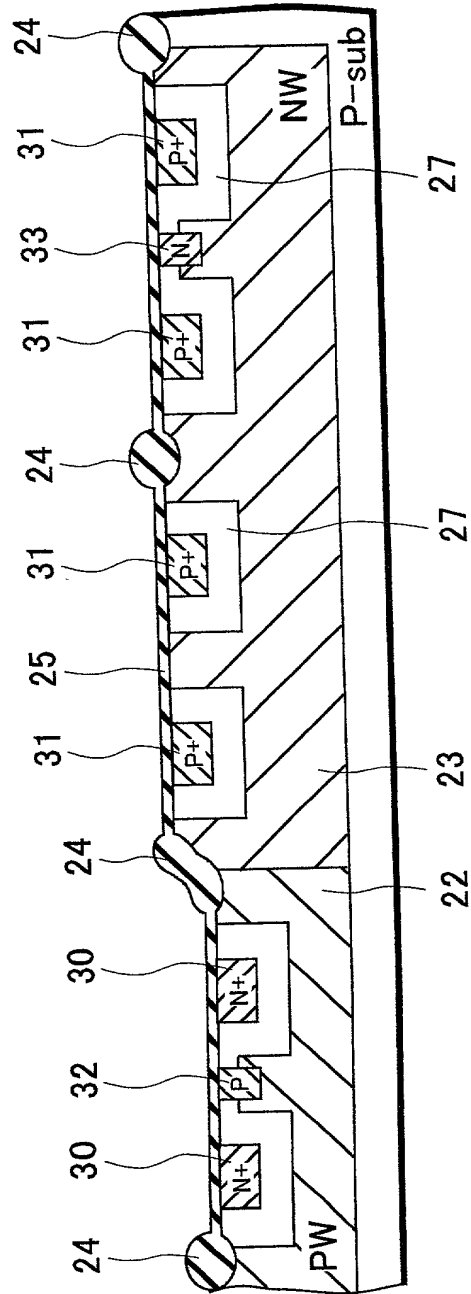


FIG. 7B







This cross-sectional view shows a semiconductor device with a substrate labeled 'P-sub'. The device features several regions: 'SPW' (Semiconductor Patterned Wafer) at the bottom left, 'SNW' (Semiconductor Patterned Wafer) at the bottom right, and 'PW' (Patterned Wafer) at the top. The device is divided into four main sections labeled 38A, 38B, 38C, and 38D. Each section contains a central region labeled 'N+' or 'P+' and is surrounded by regions labeled 'N-' or 'P-'. The regions are separated by vertical lines, and the entire structure is covered by a top layer labeled '24'. The regions are also labeled with '39' and '40' at the bottom.

[illegible]

[illegible]

This diagram shows a cross-sectional view of a semiconductor device. It features a substrate with a series of gates (30) and contacts (24, 26, 28, 32, 34, 36, 38, 40). The gates are labeled with various regions: NW, P-sub, P+, N+, and PW. The contacts are labeled with various regions: 24, 26, 28, 32, 34, 36, 38, and 40. The device is shown in a perspective view, with the gates and contacts arranged in a row.

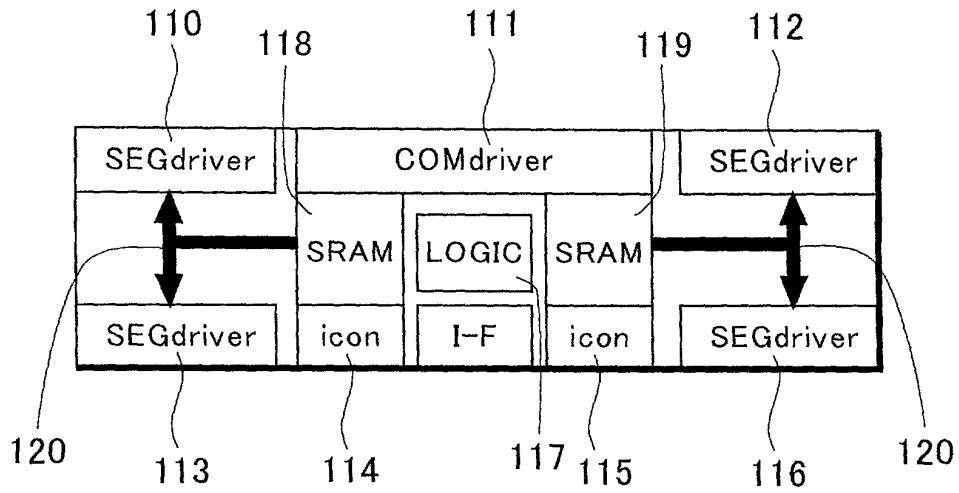
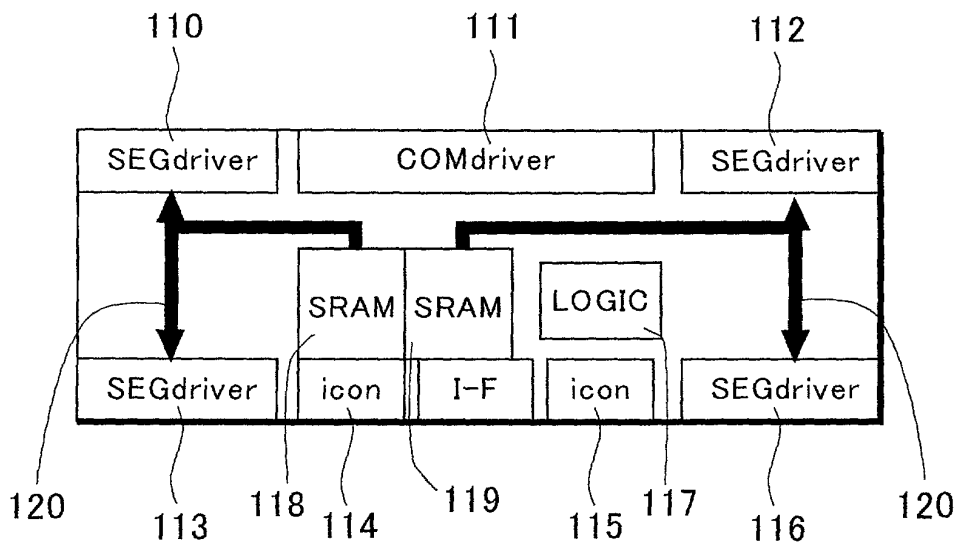
**FIG.11A****FIG.11B**

FIG. 12

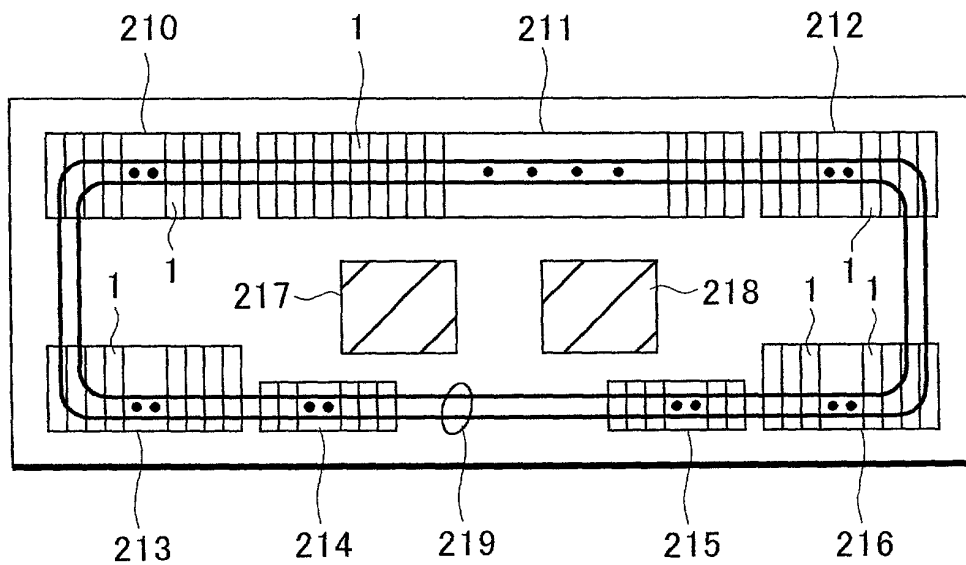
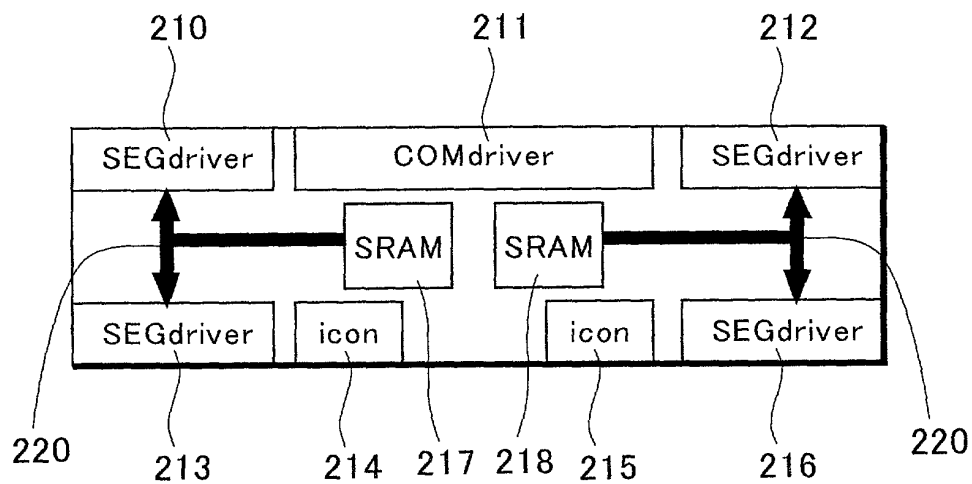
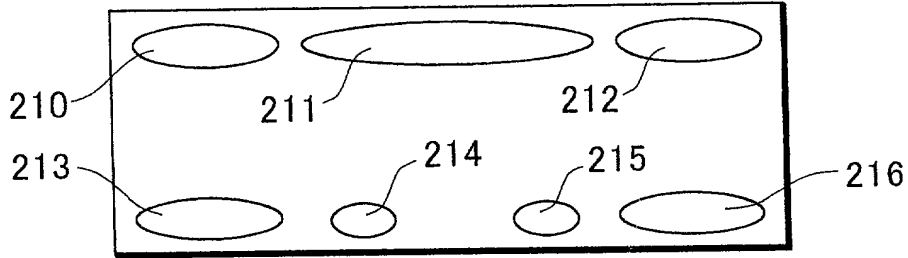


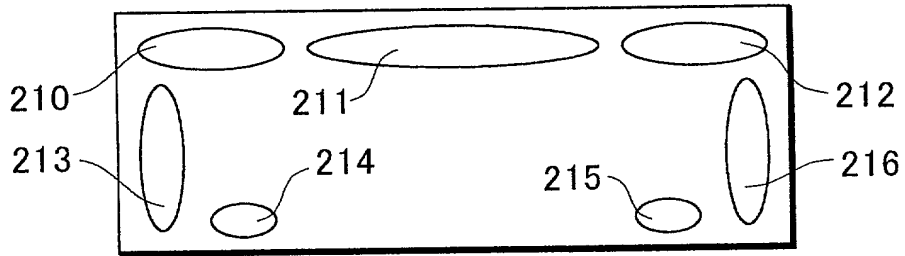
FIG. 13



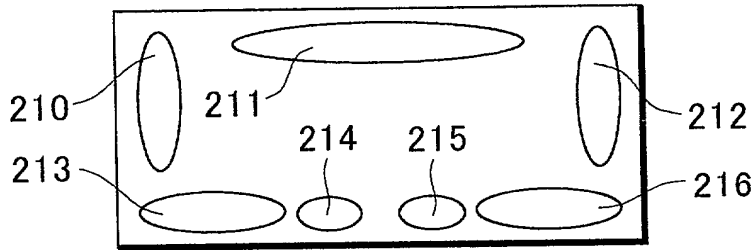
**FIG.14A**



**FIG.14B**



**FIG.14C**



**FIG.14D**

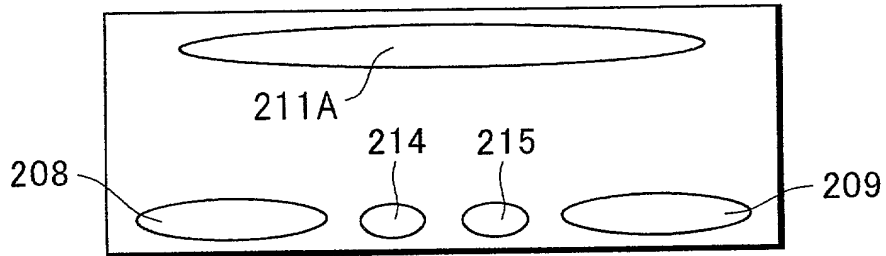


FIG. 15

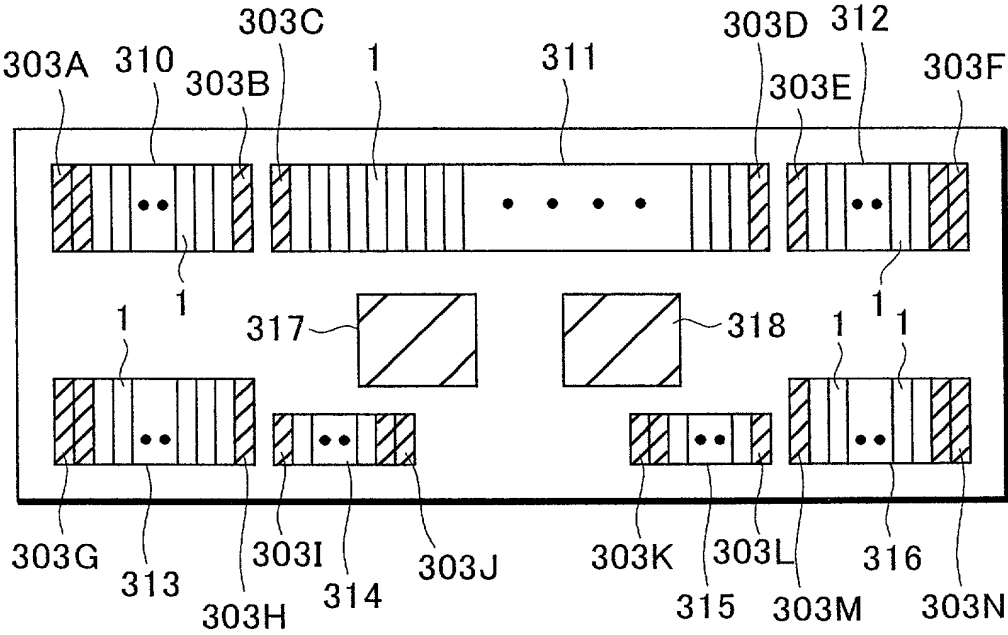
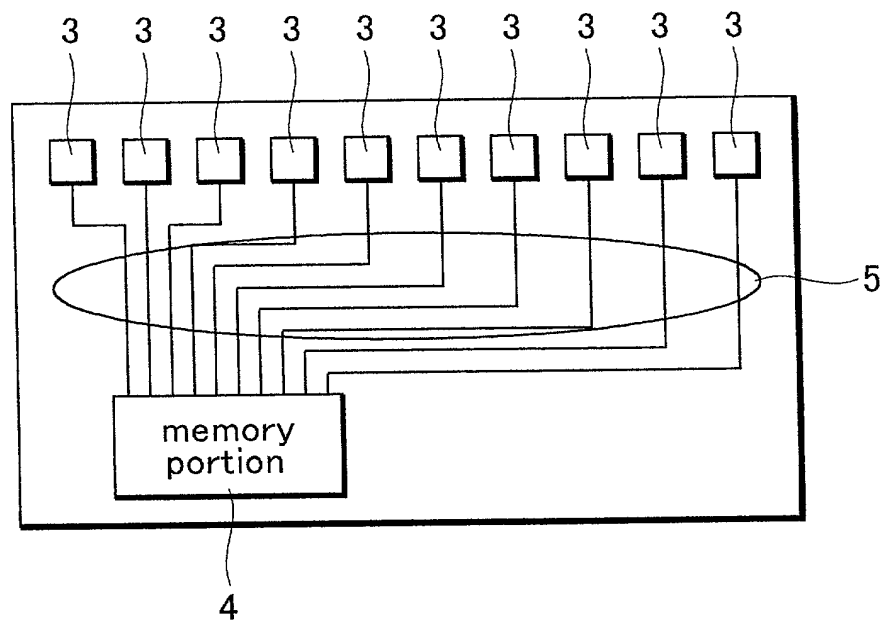
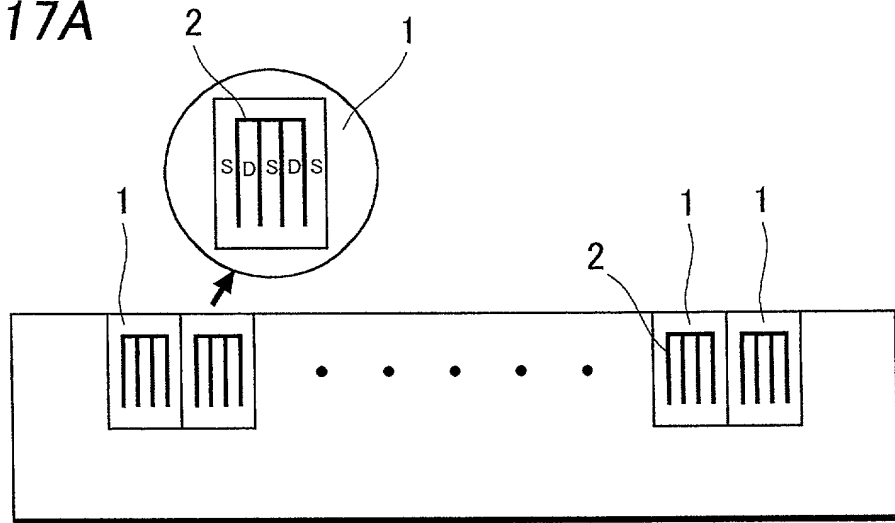


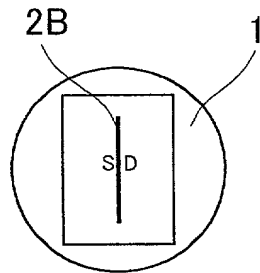
FIG. 16



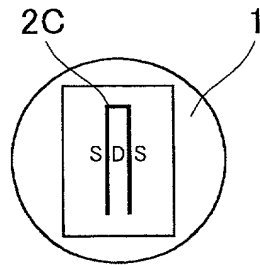
**FIG.17A**



**FIG.17B**



**FIG.17C**



**FIG.17D**

